Amendments to the Specification:

Please replace the paragraphs on page 10, lines 5-18, page 12, lines 6-16, and page 13 line 19 to page 14, line 12 in the current specification with the following new paragraphs:

Page 10, lines 5-18

> In comparison with the conventional self-routing switching element 100 of FIG. 1, two new components are overlaid on the element 100 to generate the new primitive switching element in accordance with the present invention; this structure of the new element, designated element 600 in FIG. 6, is implemented as follows: (a) there is an input for signaling using the slot signals 401-1, 401-2, 401-3, ... The sequence of slot signals is generically referred as the "slot clock" 601 in FIG. 6; and (b) there are two latch mechanisms (instead of the one mechanism engendered by latch 109 of FIG. 1) to control connection state 105, namely, one mechanism is activated for the duration of a large packet and the other mechanism for the duration of a small packet. The two mechanisms are to be referred to as "latch" and "lock", respectively. Control section 603 of switching element 600 keeps track of the status of both "latching" and "locking" and stores it in the memory register called the "latch/lock status" ~~603~~ 609. Moreover, clock counter 602 is now reset by signaling from the slot clock 601 as well as the frame clock signals 201-1, 201-2, . . . , and bit transitions from bit clock 108 still increment clock counter 602.

Page 12, lines 6-16

> As alluded to above, the scheme of packet formatting can be generalized into a recursive nested format for N packet sizes; concomitantly, there will be N levels of switching control each triggered by signaling from a different clock. Thus the latching of the connection state at each level is for the duration of a packet of the corresponding size. Take the example when there are three packet sizes: large, small, and mini. As before the frame payload 207 of a frame either contains a large packet or is partitioned into slots. Illustrated in FIG. 7, a slot now contains a slot header 701 and a slot payload. The slot payload either contains a small packet or is partitioned into mini-slots for carrying mini packets. Each mini packet arrives in synchronization with the "mini-slot clock" signal ~~710-1, 710-2, 710-3~~ 701-1, 701-2, 701-3, . . . , and so forth. FIG. 7 also depicts the relation between the slot clock signal and the mini-slot clock signal.

Page 13, line 19 to page 14, line 12

> The operational processing effected by primitive switching element 600 is as follows, with reference to the example covered by FIG. 8; in particular, it is assumed that a frame in format 300-1 serves as Input 0 on path 101-1, and a frame in format 300-2 serves as Input 1 on path 101-2. The starting point for the processing is the arrival of frame clock signal 210-1 at the input to control circuit 603. It is presumed that element 600 has synchronized with the frame clock

(107), the bit clock (108) and the slot clock (601) during prior packet/frame processing. Shift register ~~101-1~~ 102-1 receives the bit `1` from header 801-1 as its first bit. Similarly, register ~~101-2~~ 102-2 receives the bit `0` as its first bit from header 801-2. In turn, both first bits are detected by the connection state circuitry 105 in FIG. 6, which then finds the presence of a large packet and, accordingly, is committed to setting the connection state and latching it for the duration of the frame. If it is further presumed that element 600 is at the 1-st stage in the multistage switching fabric, then the D.sub.1 bit in packet header 802 is used to route frame in format 300-1. For example, if D.sub.1=0, then frame in format 300-1 is routed to Output 0; on the other hand if D.sub.1=1, then frame in format 300-1 is routed to Output 1. Since the frame-level control treats the frame 300-2 no differently from an idle expression, the frame in format 300-2 is routed to the opposite output in both cases.